AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-4 (canceled).

Claim 5 (new): An image processing device comprising:

a high-speed bus and a peripheral bus linked via a bus bridge;

a CPU arranged to carry out computations and control of image processing;

a data transceiving FIFO memory arranged to carry out transceiving of image compression data with a host device;

a frame memory arranged to store image expansion data and to display the data on a display panel; and

a compression/expansion circuit arranged to carry out compression of image expansion data and expansion of image compression data; wherein

the CPU and the frame memory are connected to the high-speed bus, and the data transceiving FIFO memory is connected to the peripheral bus.

Claim 6 (new): The image processing device according to claim 5, wherein the compression/expansion circuit is connected to the high-speed bus.

Claim 7 (new): An image processing device comprising:

a CPU-direct instruction bus, a CPU-direct data bus, and a high-speed bus;

a CPU arranged to carry out computations and control of image processing;

a ROM arranged to store a processing program of the CPU;

a RAM used as a working area for the computations carried out by the CPU;

a data transceiving FIFO memory arranged to carry out transceiving of image compression data with a host device;

a frame memory arranged to store image expansion data and to display the data on a display panel;

a compression/expansion circuit arranged to carry out compression of image expansion data and expansion of image compression data; wherein

the CPU and the ROM are connected to the CPU-direct instruction bus; the CPU, the RAM, and the frame memory are connected to the CPU-direct data bus; and the CPU and the data transceiving FIFO memory are connected to the high-speed bus.

Claim 8 (new): The image processing device according to claim 7 wherein the compression/expansion circuit is connected to the CPU-direct data bus.

Claim 9 (new): The image processing device according to claim 7, wherein the CPU-direct instruction bus includes a tightly coupled memory instruction bus.

Claim 10 (new): The image processing device according to claim 7, wherein the CPU-direct data bus includes a tightly coupled memory bus.

Claim 11 (new): The image processing device according to claim 7, wherein the high-speed includes an advanced microcontroller bus architecture.

Claim 12 (new): The image processing device according to claim 7, wherein the high-speed bus operates at a frequency of at least 75 MHz.

Claim 13 (new): The image processing device according to claim 5, wherein the high-speed bus operates at a frequency of at least 75 MHz.